

FIG. 1A

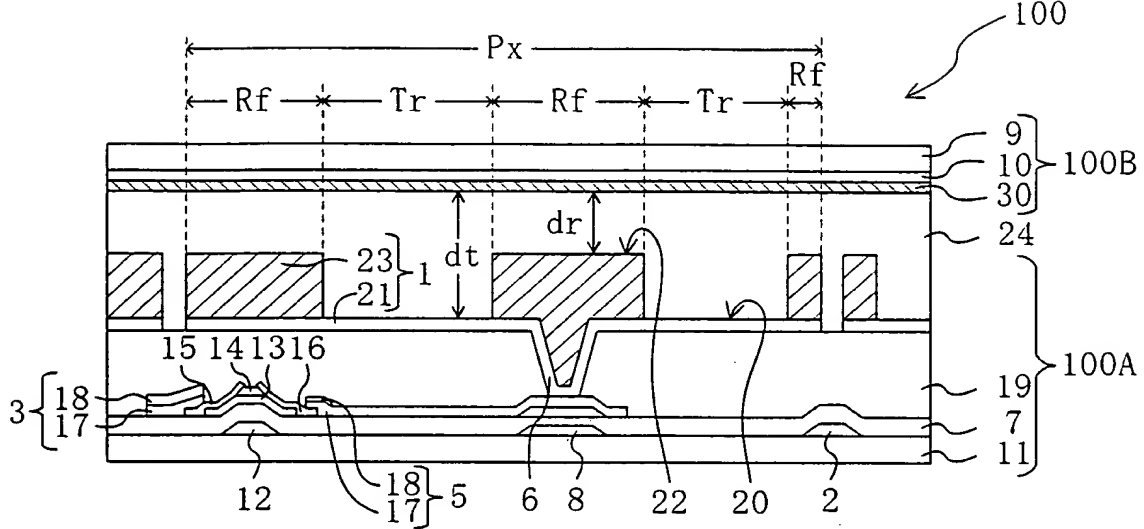


FIG. 1B

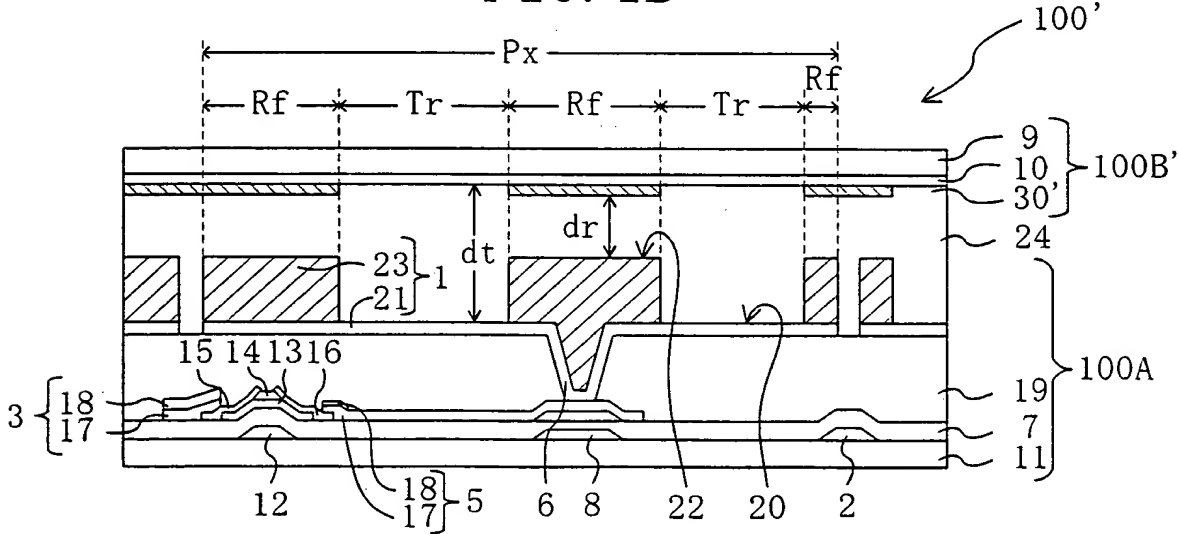
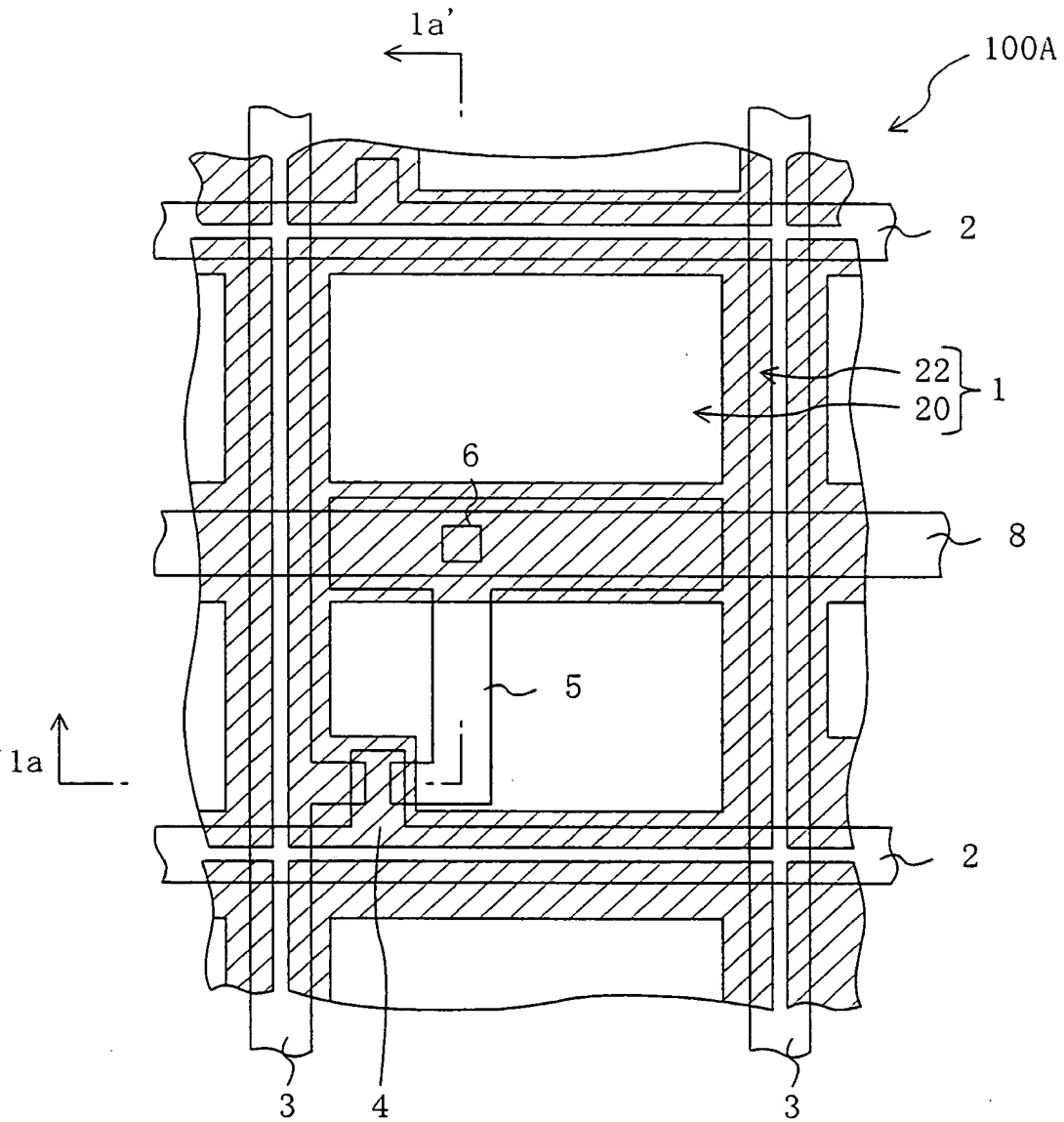


FIG. 2



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FIG. 3A

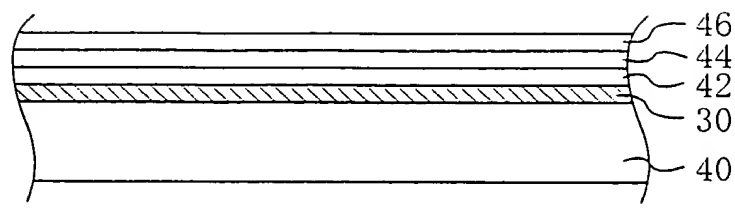


FIG. 3B

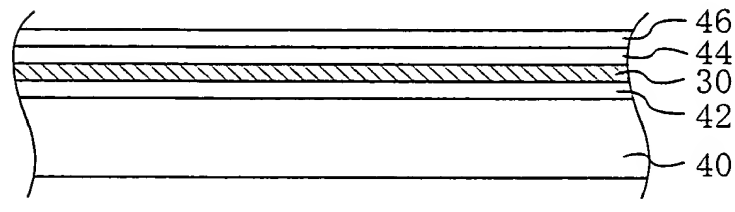


FIG. 3C

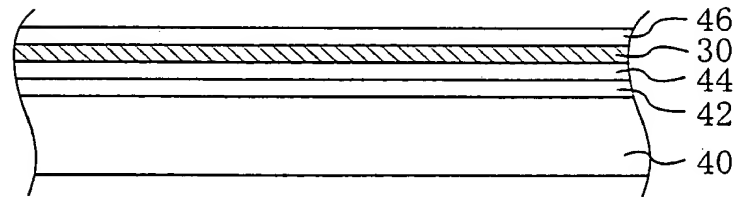


FIG. 4A

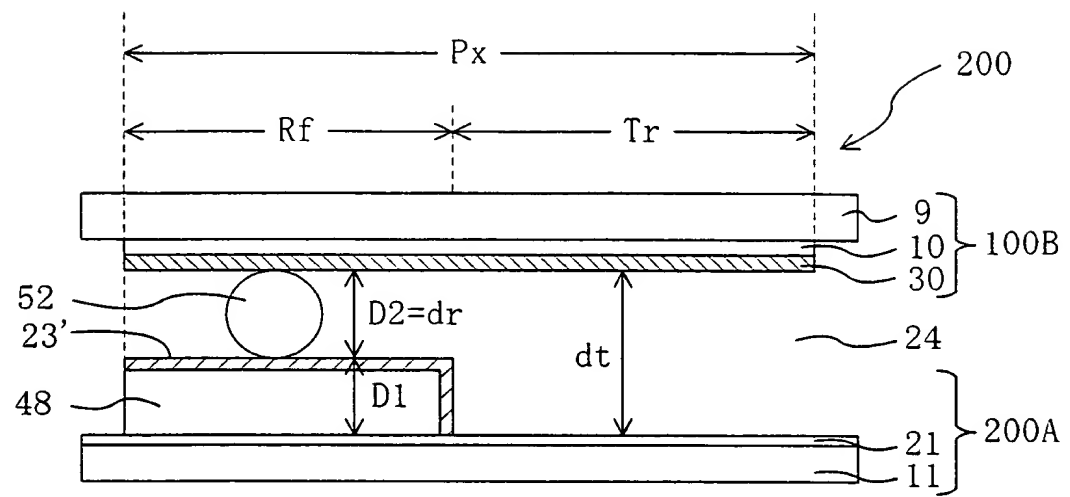


FIG. 4B

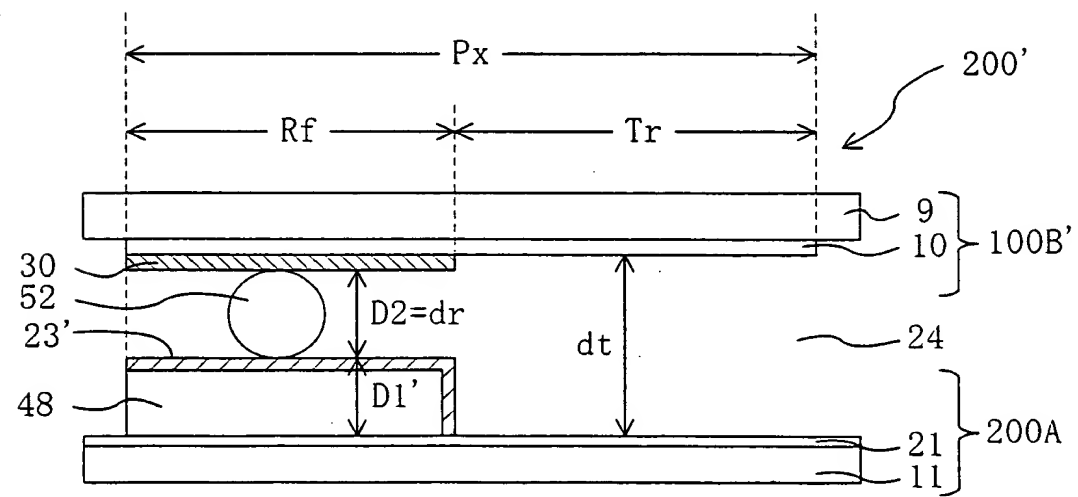


FIG. 5

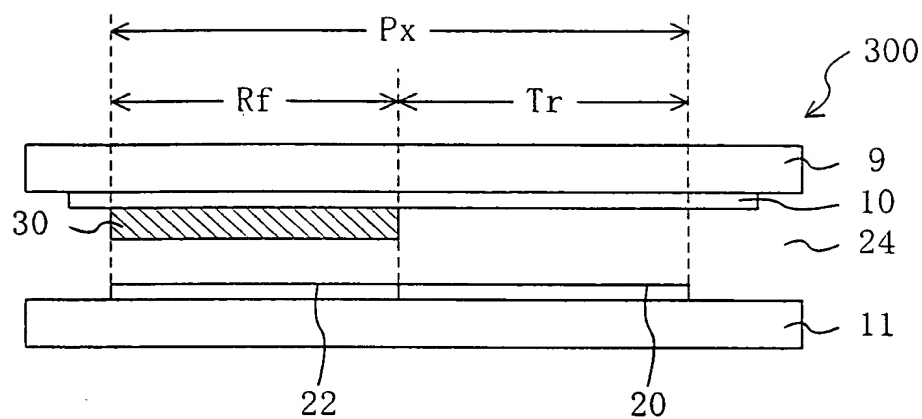


FIG. 6

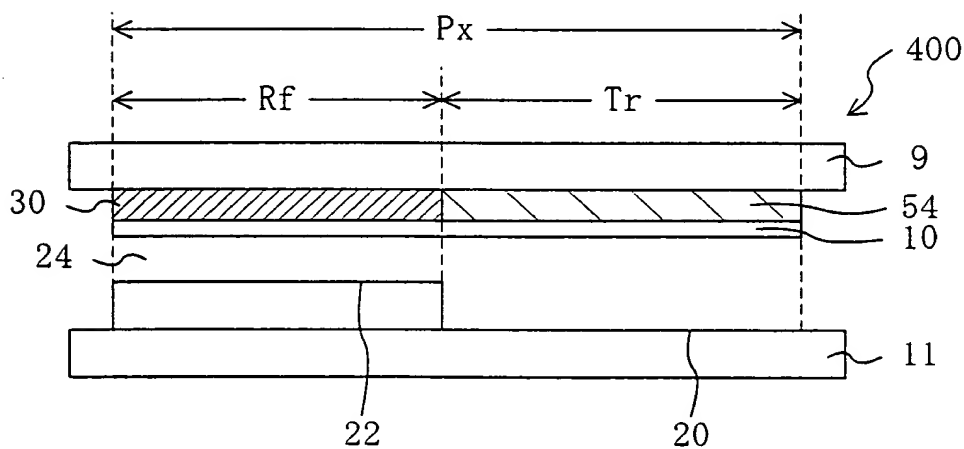


FIG. 7

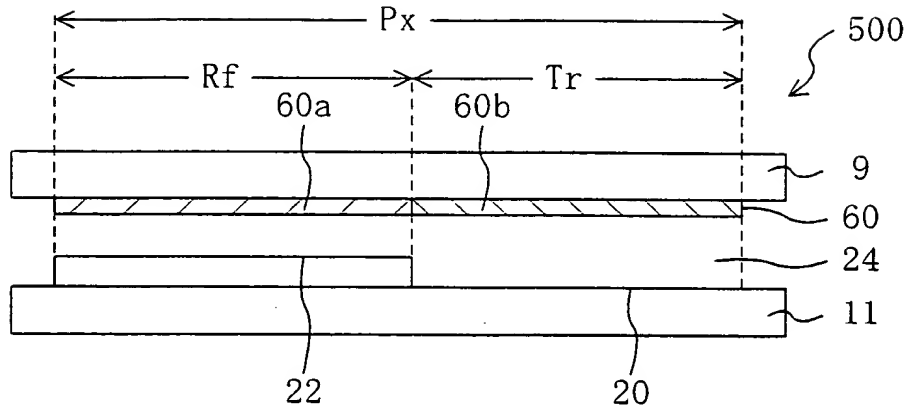


FIG. 8

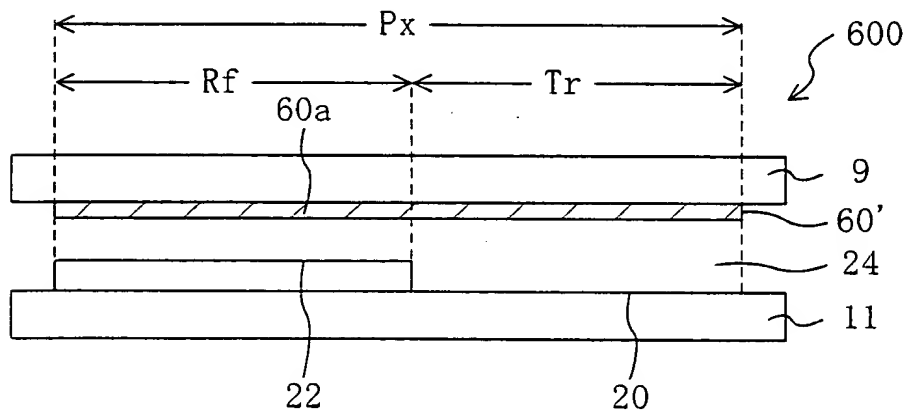


FIG. 9

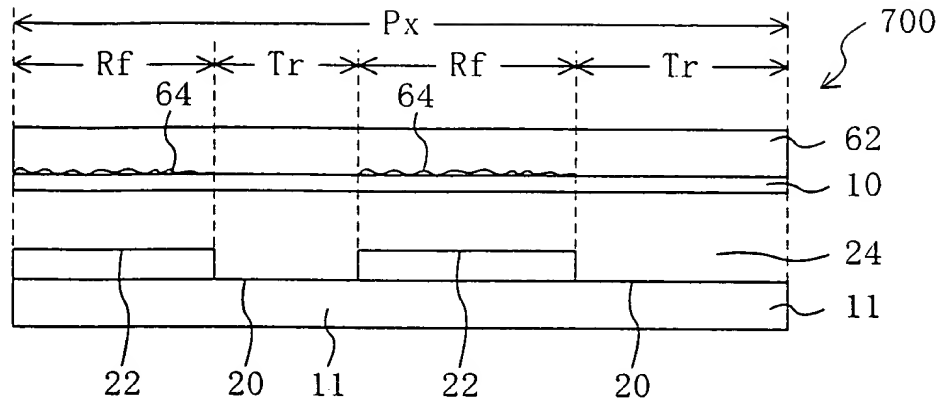


FIG. 10

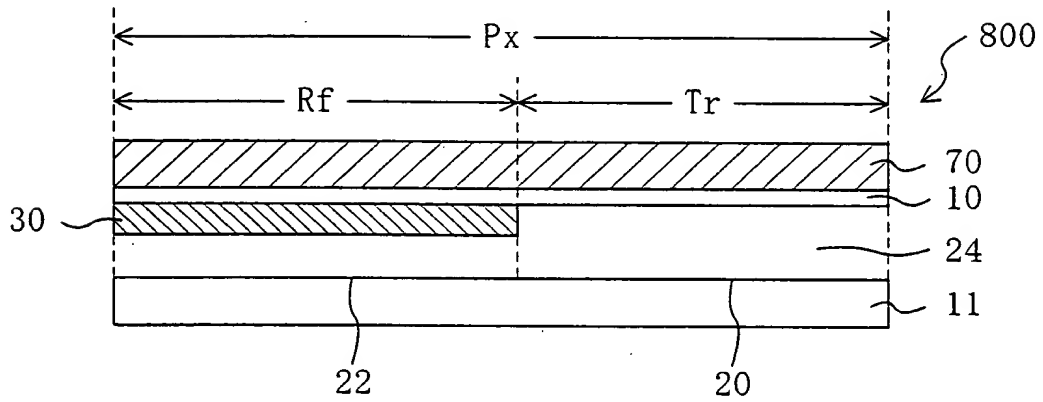
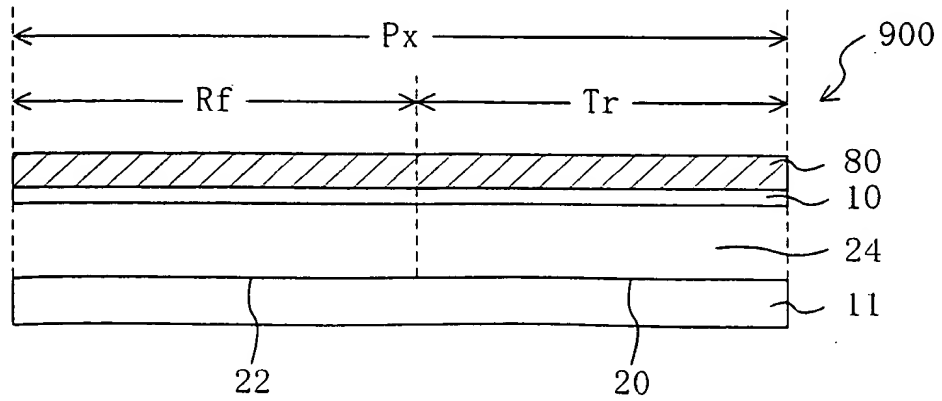


FIG. 11



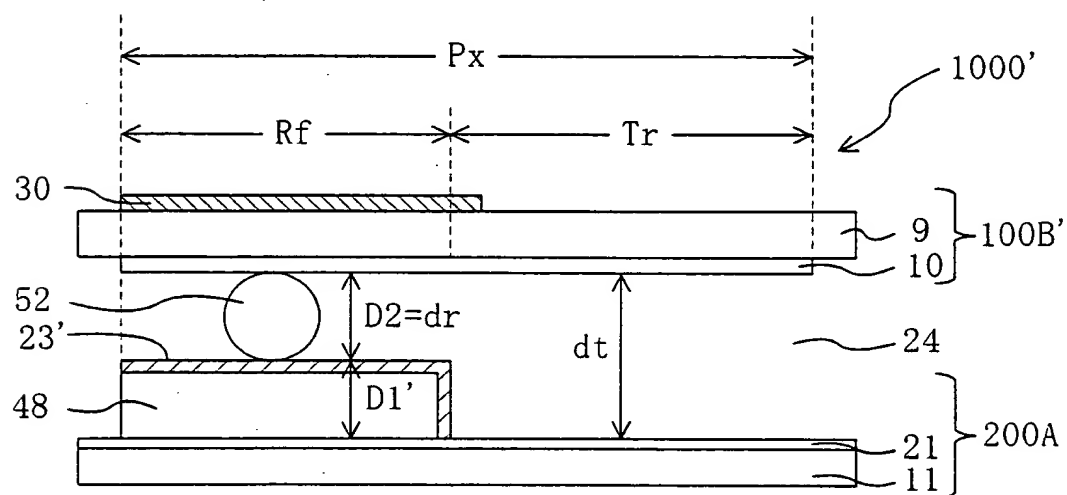


FIG. 13

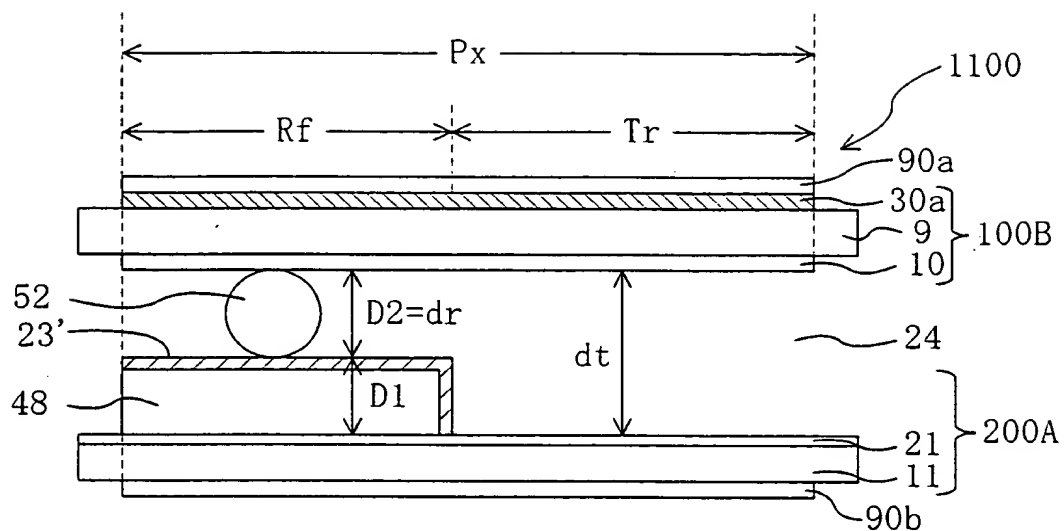


FIG. 14

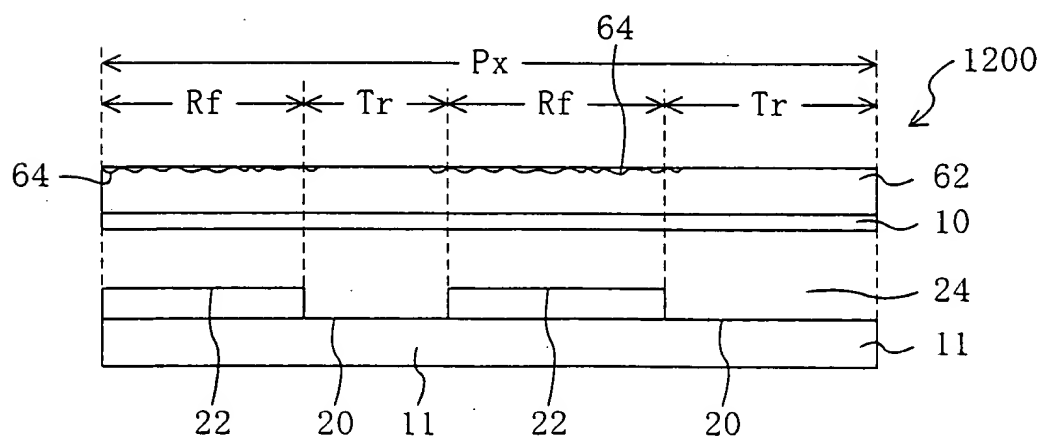
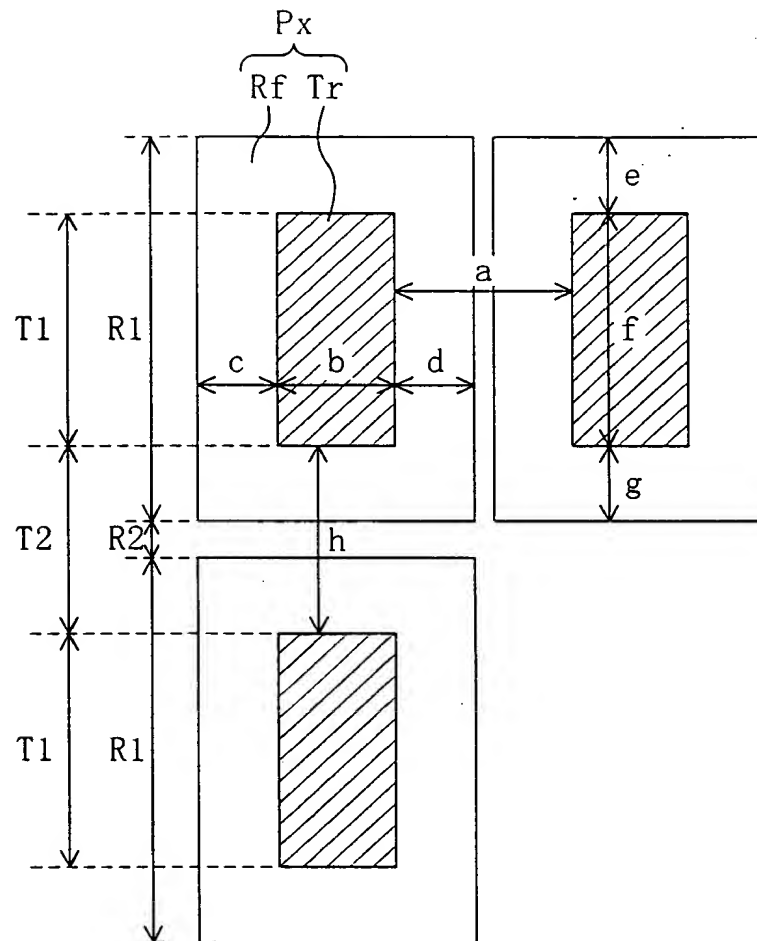


Diagram illustrating a cross-sectional view of a semiconductor device 100B. The device includes a substrate 11, a layer 20, a layer 22, a layer 24, and a layer 9. The layer 9 is divided into regions 94 and 30. The layer 10 is shown below the layer 9. Dimensions Px, Rf, and Tr are indicated. A dashed line 1300 is shown.

This diagram shows a cross-sectional view of a second embodiment of the semiconductor device. It features a substrate 100B with a top layer 9 and a bottom layer 10. A layer 24 is positioned between the substrate and a layer 11. A layer 90b is located at the bottom of the device. A layer 30 is positioned between the top layer 9 and the bottom layer 10. A layer 90a is positioned between the top layer 9 and the layer 30. A layer 94 is positioned between the top layer 9 and the layer 90a. The device is divided into two regions by a vertical dashed line: a front region (Rf) and a rear region (Tr). The total width of the device is labeled Px. The width of the front region is labeled Rf, and the width of the rear region is labeled Tr. The device is labeled 1400.

FIG. 17



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FIG. 18

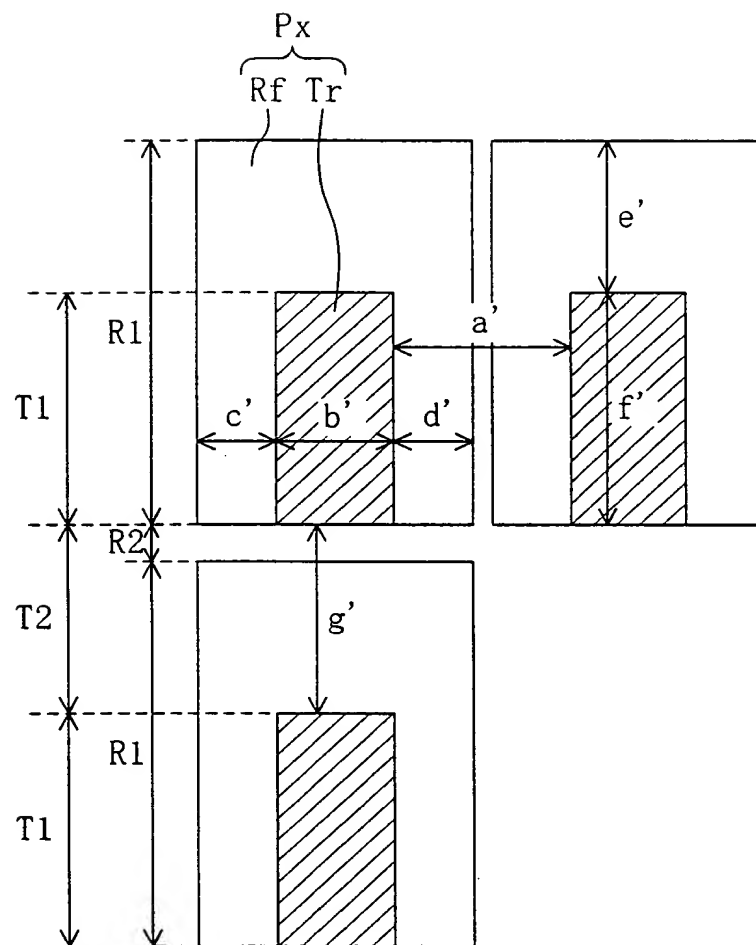


FIG. 19

